Technical Note

TN_185

What is USB Power Delivery?

Version 1.0

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This Technical Note details aspects of USB Power Delivery which uses a Type-C connector and details FTDI products which can be used with Type-C.

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1 Introduction

USB Power Delivery (PD) is a USB power standard that allows higher power to be sinked (from the USB Host) or sourced (from the USB Device) using a Type-C USB cable.

This has the advantages of sinking higher power to be used with additional external circuits and providing power to the USB Host to allow for charging as an example. Without USB PD support only a USB Host is allowed to provide power to the USB device.

Power can be supplied at the same time as data communication using the USB Type-C connector which is necessary for USB PD and is discussed in this document. FTDI PD products offer data communication like UART, SPI, I2C, FIFO, etc alongside PD.

Table 1.1 shows a comparison of the maximum power possible for more recent USB specifications.

Specification	Max Voltage (V)	Max Current	Max Power (W)
USB 2.0	5	500mA	2.5
USB 3.x	5	900mA	4.5
USB BC 1.2	5	1.5A	7.5
USB PD 3.0	20	5A	100
USB PD 3.1	48	5A	240

Table 1.1 USB Power Comparison

USB 2.0 and 3.0 power supply is simple as the USB Host can only supple 5V/500mA and 5V/900mA maximum respectively.

USB Battery Charge 1.2 is detailed in AN_175 Battery Charger Detection over USB with FT-X Devices.

USB PD 3.0 supports 5V/3A, 9V/3A, 12V/3A, 15V/3A, 20V/3A and more Power Delivery Objects (PDOs) as sink or source as shown in Table 1.2.

Power Output (W)	Current (A)			
	5V	9V	15V	20V
0.5-15	0.1 to 3A			
15-27		1.7-3A		
27-45			1.8-3A	
45-60				2.25-3A
60-100				3-5A*

Table 1.2 USB PD 3.0 Power Ranges

FTDI offer product solutions USB PD 3.0, so this Technical Note concentrates on the features of USB PD 3.0.

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*** Note** special cables that are electronically marked by employing a chip inside to allow for 5A to be delivered at 20V. FTDI PD products can offer a PD **sink** profile for 20V/5A. A PD source profile for 20V/5A is not supported because the IC needs to enable and initiate Vconn which is not currently supported.

FTDI plan to have USB PD 3.1 product support on our roadmap which will also include 48V/5A power.

Both USB Host and device must support PD feature for this increased power. If a PC or laptop does not support USB PD then the default power will be used.

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2 USB Type-C Connector

A Type-C to Type-C cable is mandatory for USB PD to operate as shown in Figure 2.1.

Figure 2.1 USB Type-C to Type-C Cable

If at one end of the cable is a Type-A connector as shown in Figure 2.2 then PD negotiation is not possible as the Configuration Channel (CC) lines are not available which are used for the PD communication. This is discussed in section 3.4.

Figure 2.2 USB Type-C to Type-A Cable

An electronically marked Type-C cable is used when 20V/5A power is required as shown in Figure 2.3. This contains an IC inside the cable which is used for the 5A power negotiation.

Figure 2.3 USB Type-C to Type-C 5A Cable

A goal of USB Power Delivery technology is to reduce e-waste. Each USB Type-C device will not need its own specific cable. You should be able to use the same cable for all your devices. It will eliminate the need to get a new one each time you upgrade or get a new device.

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3 USB Type-C Connector Pinout

This section shows the Type-C plug / receptacle pinout and signal names for reference.

Figure 3.1 shows the USB Type-C receptacle pinout which is usually on the USB Host side, or what a USB Type C cable from the USB device connects to.

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1−	VBUS	CC1	D+	D−	SBU1	VBUS	RX2−	RX2+	GND
GND	RX1+	RX1−	VBUS	SBU2	D−	D+	CC2	VBUS	TX2−	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

Figure 3.1 USB Type-C Receptacle (Front View)

Figure 3.2 shows the USB Type-C plug pinout. This plug would connect directly to the USB Type C receptacle on the USB Host.

A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
GND	RX2+	RX2−	VBUS	SBU1	D−	D+	CC	VBUS	TX1−	TX1+	GND
GND	TX2+	TX2−	VBUS	VCONN			SBU2	VBUS	RX1−	RX1+	GND
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12

Figure 3.2 USB Type-C Plug Interface (Front View)

Figure 3.3 shows how the USB Type-C connectors physically look with the receptacle on the left and the plug on the right.

Figure 3.3 USB Type-C Connectors

Note that inside a USB Type-C to Type-C cable there is only one CC wire.

3.1 Data Signals

There are two groups of signals for USB 2.0 and USB 3.0 data communication. These signals are differential.

USB 2.0: D+, D-

USB 3.0: TX1+, TX1-, TX2+, TX2-, RX1+, RX1-, RX2+, RX2-

3.2 Power Signals

The main power signals are GND and VBUS.

The maximum VBUS voltage is according to Table 1.1.

VCONN is also a power signal used to power the IC inside the electronically marked Type-C cable. This is used when 20V/5A power is required.

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3.3 Sideband Use Signals

There are the Sideband Use pins (SBU1 and SBU2). These are used to carry Alternate Modes that allow the Type-C connector to transport other high-speed protocols, such as DisplayPort and Audio Accessory Mode. These are not used by FTDI products so will not be discussed in this document.

3.4 Configuration Channels (CC1/2)

The CC Pins are for cable attach/removal detection, orientation, role detection and current mode.

Cable detection occurs when one of the two CC lines pulls down. This is monitored by the host.

Cable orientation is based on which CC line pulls down.

The values of resistance determine the current-carrying capability by sensing the voltage at the center tap of the voltage divider.

A standard USB Type C cable only has one CC wire inside as shown in Figure 3.4.

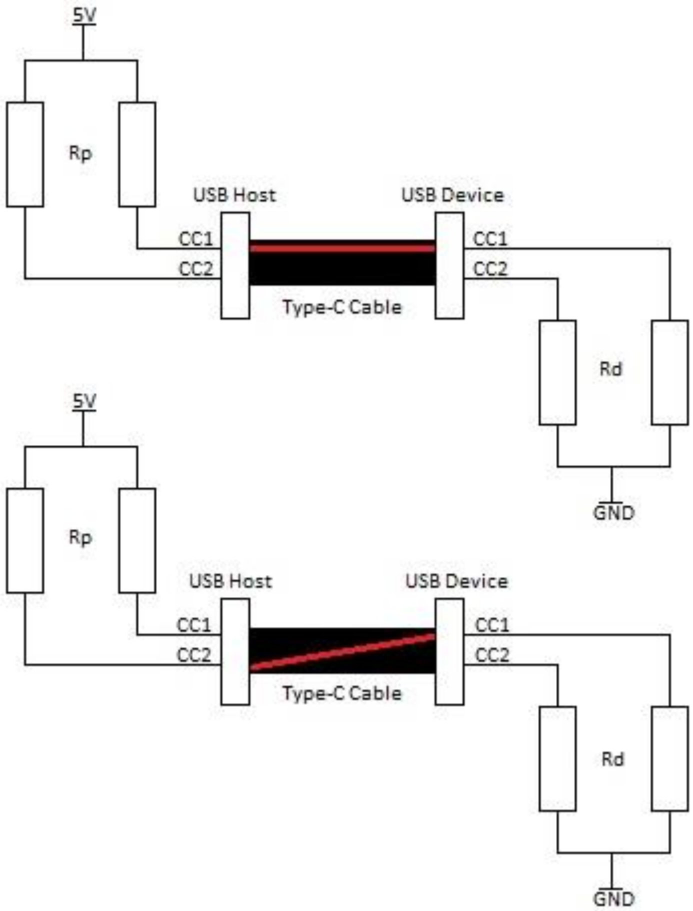

Figure 3.4 CC Wire Orientation

The Host pulls up the CC1 and CC2 pins through the Rp resistors, but the device pulls them down through Rd.

If no cable is attached, the source sees a logic high at CC1 and CC2 pins.

Connecting the USB Type-C cable creates a current path from the 5V supply to ground. Since there is only one CC wire inside the USB Type-C cable, only one current path is formed.

For example, in the upper part of Figure 3.4, the CC1 pin of the Host is connected to the CC1 pin of the device. The Host CC1 pin will have a voltage lower than 5V but the device CC2 pin will be still at the logic high. Therefore, monitoring the voltage on the host CC1 and CC2 pins, cable attachment and orientation can be determined.

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In addition to the cable orientation, the Rp-Rd path is used as a way of communicating information about the source current capabilities.

The power consumer (Device) monitors the voltage on the CC line. When the voltage on the CC line has its lowest value (about 0.41V), the source can provide the default USB power which is 500mA and 900mA for the USB 2.0 and USB 3.0 respectively.

When the CC line voltage is about 0.92V, the source can provide a current of 1.5A.

The highest CC line voltage, which is about 1.68V corresponds to the source current capability of 3 A.

The VCONN signal is used with special cables that are electronically marked by employing a chip inside to allow for 5A to be delivered.

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4 USB 2.0 (no PD) ICs with Type-C

FTDI USB 2.0 High and Full Speed ICs do not support PD but can be used with a Type-C Connector. See TN_181 Type-C USB Connectors with FTDI Products for more details.

This mainly involves pulling the CC lines low via a 5k1 resistor.

Note that a maximum of 5V/500ma can only be sinked from the USB Host with this configuration.

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5 USB 3.x (no PD) ICs with Type-C

FTDI USB 3.0 SuperSpeed ICs were not designed with USB Power Delivery (PD) but can also be used with a Type-C connector.

Our SuperSpeed modules only contain a Micro-USB3.0 receptacle and are not built with a Type-C connector.

To use the FT60x with a Type-C connector there could be 2 application configurations:

1. An application to use Type-C plug with captive cable. In this scenario the user can choose 1 set of signals and connect to the FT60x directly (SS MUX not required).
2. An application to use Type-C receptacle and use generic full-set Type-C cable to connect the host (DFP) and device (UFP).
   In this scenario a SS MUX with CC control logic is required to be put between Type-C receptacle and FT60x. One good example is TI's HD3SS3220. Refer to reference schematics here and replace J3 USB3_TypeA_Connector portion with FT60x.

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6 FTDI PD Capable Products with Type-C

The FT23xHP/FT223xHP/FT423xHP products offer the same functionality as the original FT232H/FT2232H/FT4232H products. They can be used for UART, bit bang, I2C/SPI via MPSSE, etc. However, these HP products support USB PD as well.

Device	Description
FT232HP	USB to Single Channel Serial UART/FIFO/JTAG/SPI/I2C with one PD Port.
FT233HP	USB to Single Channel Serial UART/FIFO/JTAG/SPI/I2C with two PD Ports.
FT2232HP	USB to Dual Channel Serial UART/FIFO/JTAG/SPI/I2C with one PD Port.
FT2233HP	USB to Dual Channel Serial UART/FIFO/JTAG/SPI/I2C with two PD Ports.
FT4232HP	USB to Quad Channel Serial UART/JTAG/SPI/I2C with one PD Port.
FT4233HP	USB to Quad Channel Serial UART/JTAG/SPI/I2C with two PD Ports.

Table 6.1 HP Product Summary

All products in Table 6.1 have USB PD port 1 which also carries the USB data communication. This can switch between the roles of sinking power from the host to power the peripheral and sourcing power to charge the host computer. This is known as dual-role power (DRP) which can operate as either a sink or source.

The products in Table 6.1 with two PD ports have PD Port 2 which is a power sink port that can be used to connect an external power source or charger. This can provide power to the peripheral board as well as charging the host via PD port 1.

6.1 Modules

Development modules are available from FTDI as per Table 6.2.

Module	Description	Notes
UMFT233HPEV	USB High Speed Single Channel Serial/FIFO bridge evaluation module with two Type-C USB PD Ports.	Contains external EEPROM for PDO profile programming. Contains FT233HPQ but can be used to evaluate FT232HP and FT233HP.
UMFT4233HPEV	USB High Speed Quad Channel Serial bridge evaluation module with two Type-C USB PD Ports.	Contains external EEPROM for PDO profiles. Contains FT4233HPQ but can be used to evaluate FT2232HP, FT2233HP, FT4232HP and FT4233HP.
UMFT232HPEV-S	USB High Speed single channel serial bridge development module with one type-C PD Port with only sink capabilities that support USB Bus power option 5V3A.	No external EEPROM for PDO profiles. Sink only at 5V3A. Can be used only to evaluate FT232HPQ.
UMFT233HPEV-SD	USB High Speed single channel serial bridge development module with two type-c USB PD Ports with	Contains external EEPROM for PDO profile programming.

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Module	Description	Notes
	only sink capabilities that support USB Bus power option (5V3A,9V3A,12V3A,15V3A,20V3A).	Sink only configuration. Contains FT233HPQ but can be used to evaluate FT232HP and FT233HP.

Table 6.2 HP Module Summary

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7 FTDI PDO Profiles

The default profile with no changes to the external EEPROM is sink at 5V/3A. So, this means that the USB Host gives this supply from VBUS.

By using an external EEPROM, it is possible to change the PD configuration based for specific use cases, such as USB Port 1 sink, USB Port 1 sink or source, and PD charge through from USB Port 2 to USB Port 1 as some examples. The PDO voltage/current profiles can also be customized.

This can be configured via the [FT_PROG]() EEPROM programming utility.

Note that other device specific configurations can be made which don't relate to PD so are not covered in this document. This is shown in the section above 'Power Delivery' as shown in Figure 7.1.

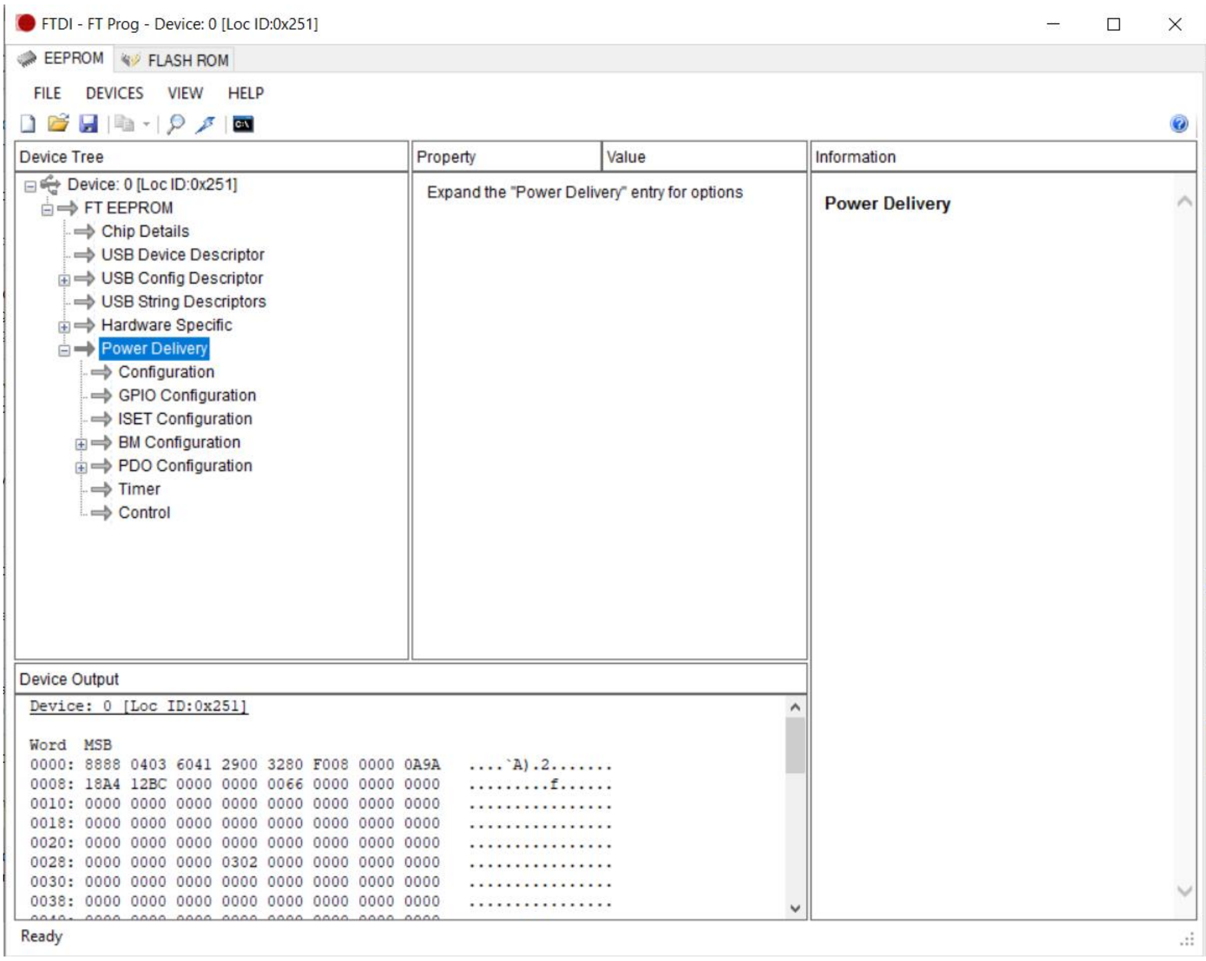

Figure 7.1 USB Type-C Connectors

The following two documents give details on the configuration options:

- [AN 551 FT4232HP FT2232HP FT232HP Configuration Guide]()
- [AN 449 FT4233HP FT2233HP FT233HP FT4232HP FT2232HP FT232HP DCDC Power Delivery Application Note]()

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7.1 Sample PDO Profiles

These examples show partial FT_PROG .xml configurations for 9V source profile and for PD Pass-through function enable. These are example profiles which would allow the FTDI IC to provide charge to the PC of the USB Host.

Note that only the <Power_Delivery> section of the .xml is shown. Other aspects of the .xml which do not relate to PD are not shown to reduce the size of the document. With a text editor, the partial .xml can be applied to an existing .xml which can be obtained by using FT_PROG to 'Save as a Template'.

These examples are applied to the UMFT233HPEV with an external power meter to help measure the power supplied to or from the USB port.

Figure 7.2 UMFT233HPEV with external power meter

7.1.1 USB PD Port 1 9V / 3A Source

The partial .xml is shown in Appendix A – 233_DCin_PD1Dual_9V.xml.
The key aspects of the configuration are shown below which configures PD1 to source 9V/3A to the USB Host.

If users want to control load switch for different PDO profiles, they must set GPIOs.
If negotiated power of 9V (PDO2) is successful, GPIO0 and GPIO1 go high and LED D1 and LED D2 light.

FT_Prog settings should match the hardware design.

PDO Source profile:

```
<BM_PDO_Source>
        <pdo1ma>3000</pdo1ma>
        <pdo1mv>5000</pdo1mv>
        <pdo2ma>3000</pdo2ma>
        <pdo2mv>9000</pdo2mv>
```

Use three GPIOs to control the power:

```
<GPIO_Configuration>
      <count>2</count>
      <gpio1>0</gpio1>
      <gpio2>1</gpio2>
```

GPIO pin configuration:

```
<GPIO_BM_PDO1>
        <GPIO1>Drive Hi</GPIO1>
        <GPIO2>Drive Low</GPIO2>
```


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```
<GPIO_BM_PDO2>
        <GPIO1>Drive Hi</GPIO1>
        <GPIO2>Drive Hi</GPIO2>
```

7.1.2 USB PD2 to USB PD1 Pass Through

The partial .xml is shown in Appendix B – PassThrough.xml.

The key aspects of the configuration are shown below which allows pass through of negotiated PD profile from USB PD2 (e.g., PD charger) to USB PD1 (USB Host). Also note that in passthrough mode, the FTDI device acts as the bridge that facilitate the USB host that is attached to PD1 to negotiate PD profile directly with charger, so only the default 5V 3A sink and source PDOs are required in the EEPROM.

2 GPIOs (GPIO3 and GPIO4) are used to control the load switch to achieve the pass through.

Once the negotiated power profile is successful, GPIO3 and GPIO4 go high with LED D4 and LED D5 lighting.

FT_Prog settings should match the hardware design.

Sink Request Power Role Swap:

```
<srprs>true</srprs>
```

Sink Accept Power Role Swap:

```
<srapprs>true</srapprs>
```

Pass Through:

```
<passthru>true</passthru>
```

PDO Sink:

```
<PDO_Configuration>
      <BM_PDO_Sink>
        <pdo1ma>3000</pdo1ma>
        <pdo1mv>5000</pdo1mv>
```

PDO Source:

```
<BM_PDO_Source>
        <pdo1ma>3000</pdo1ma>
        <pdo1mv>5000</pdo1mv>
```

Use three GPIOs to control the power:

```
<GPIO_Configuration>
      <count>3</count>
      <gpio1>4</gpio1>
      <gpio2>0</gpio2>
      <gpio3>3</gpio3>
```

ISET pins are used to indicate the power profile being used when in sink:

```
<ISET_Configuration>
      <iset1>6</iset1>
      <iset2>6</iset2>
      <iset3>6</iset3>
```

GPIO pin configuration:

```
<BM_Configuration>
      <GPIO_BM_PDO1>
        <GPIO1>Drive Hi</GPIO1>
        <GPIO2>Drive Low</GPIO2>
        <GPIO3>Drive Hi</GPIO3>
```


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Please note the following points with the pass through example:

1. The adapter (charger) which connected to PD2 port must support PD functionality. The device which is connected to PD1 port also should support PD functionality.
2. Jumpers on the UMFT4233HPEV should be configured as shown in Figure 7.3. You can refer to the module datasheet for more information.

Figure 7.3 EV Jumper Configuration

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8 Conclusion

This Technical Note has shown aspects of USB Power Delivery which uses a Type-C connector and details FTDI products which can be used with Type-C connectors. Some sample PD profiles are given.

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Appendix A – 233_DCin_PD1Dual_9V.xml


```
<Power_Delivery>
    <Configuration>
      <srprs>true</srprs>
      <srapprs>true</srapprs>
      <srrprs>false</srrprs>
      <saprs>false</saprs>
      <vconns>false</vconns>
      <passthru>false</passthru>
      <extmcu>false</extmcu>
      <pd2en>false</pd2en>
      <pd1autoclk>false</pd1autoclk>
      <pd2autoclk>false</pd2autoclk>
      <useefuse>true</useefuse>
      <extvconn>false</extvconn>
    </Configuration>
    <GPIO_Configuration>
      <count>2</count>
      <gpio1>0</gpio1>
      <gpio2>1</gpio2>
      <gpio3>N/A</gpio3>
      <gpio4>N/A</gpio4>
      <gpio5>N/A</gpio5>
      <gpio6>N/A</gpio6>
      <gpio7>N/A</gpio7>
      <pd1lden>2</pd1lden>
      <pd2lden>N/A</pd2lden>
      <dispin>5</dispin>
      <disenbm>Drive Hi</disenbm>
      <disdisbm>Drive Low</disdisbm>
      <ccselect>N/A</ccselect>
    </GPIO_Configuration>
    <ISET_Configuration>
      <iset1>N/A</iset1>
      <iset2>N/A</iset2>
      <iset3>N/A</iset3>
      <extiset>false</extiset>
      <isetpd2>false</isetpd2>
      <iseten>false</iseten>
    </ISET_Configuration>
    <BM_Configuration>
      <GPIO_BM_PDO1>
        <GPIO1>Drive Hi</GPIO1>
        <GPIO2>Drive Low</GPIO2>
        <GPIO3>Don't Care</GPIO3>
        <GPIO4>Don't Care</GPIO4>
        <GPIO5>Don't Care</GPIO5>
        <GPIO6>Don't Care</GPIO6>
        <GPIO7>Don't Care</GPIO7>
      </GPIO_BM_PDO1>
      <GPIO_BM_PDO2>
        <GPIO1>Drive Hi</GPIO1>
        <GPIO2>Drive Hi</GPIO2>
        <GPIO3>Don't Care</GPIO3>
        <GPIO4>Don't Care</GPIO4>
        <GPIO5>Don't Care</GPIO5>
        <GPIO6>Don't Care</GPIO6>
        <GPIO7>Don't Care</GPIO7>
      </GPIO_BM_PDO2>
      <GPIO_BM_PDO3>
        <GPIO1>Don't Care</GPIO1>
```


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```
        <GPIO2>Don't Care</GPIO2>
        <GPIO3>Don't Care</GPIO3>
        <GPIO4>Don't Care</GPIO4>
        <GPIO5>Don't Care</GPIO5>
        <GPIO6>Don't Care</GPIO6>
        <GPIO7>Don't Care</GPIO7>
      </GPIO_BM_PDO3>
      <GPIO_BM_PDO4>
        <GPIO1>Don't Care</GPIO1>
        <GPIO2>Don't Care</GPIO2>
        <GPIO3>Don't Care</GPIO3>
        <GPIO4>Don't Care</GPIO4>
        <GPIO5>Don't Care</GPIO5>
        <GPIO6>Don't Care</GPIO6>
        <GPIO7>Don't Care</GPIO7>
      </GPIO_BM_PDO4>
      <GPIO_BM_PDO5>
        <GPIO1>Don't Care</GPIO1>
        <GPIO2>Don't Care</GPIO2>
        <GPIO3>Don't Care</GPIO3>
        <GPIO4>Don't Care</GPIO4>
        <GPIO5>Don't Care</GPIO5>
        <GPIO6>Don't Care</GPIO6>
        <GPIO7>Don't Care</GPIO7>
      </GPIO_BM_PDO5>
      <GPIO_BM_PDO6>
        <GPIO1>Don't Care</GPIO1>
        <GPIO2>Don't Care</GPIO2>
        <GPIO3>Don't Care</GPIO3>
        <GPIO4>Don't Care</GPIO4>
        <GPIO5>Don't Care</GPIO5>
        <GPIO6>Don't Care</GPIO6>
        <GPIO7>Don't Care</GPIO7>
      </GPIO_BM_PDO6>
      <GPIO_BM_PDO7>
        <GPIO1>Don't Care</GPIO1>
        <GPIO2>Don't Care</GPIO2>
        <GPIO3>Don't Care</GPIO3>
        <GPIO4>Don't Care</GPIO4>
        <GPIO5>Don't Care</GPIO5>
        <GPIO6>Don't Care</GPIO6>
        <GPIO7>Don't Care</GPIO7>
      </GPIO_BM_PDO7>
      <VSET0V>
        <GPIO1>Drive Low</GPIO1>
        <GPIO2>Drive Low</GPIO2>
        <GPIO3>Don't Care</GPIO3>
        <GPIO4>Don't Care</GPIO4>
        <GPIO5>Don't Care</GPIO5>
        <GPIO6>Don't Care</GPIO6>
        <GPIO7>Don't Care</GPIO7>
      </VSET0V>
      <VSAFE5V>
        <GPIO1>Drive Hi</GPIO1>
        <GPIO2>Drive Low</GPIO2>
        <GPIO3>Don't Care</GPIO3>
        <GPIO4>Don't Care</GPIO4>
        <GPIO5>Don't Care</GPIO5>
        <GPIO6>Don't Care</GPIO6>
        <GPIO7>Don't Care</GPIO7>
      </VSAFE5V>
    </BM_Configuration>
    <PDO_Configuration>
```


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```
    <BM_PDO_Sink>
      <pdo1ma>3000</pdo1ma>
      <pdo1mv>5000</pdo1mv>
      <pdo2ma>0</pdo2ma>
      <pdo2mv>0</pdo2mv>
      <pdo3ma>0</pdo3ma>
      <pdo3mv>0</pdo3mv>
      <pdo4ma>0</pdo4ma>
      <pdo4mv>0</pdo4mv>
      <pdo5ma>0</pdo5ma>
      <pdo5mv>0</pdo5mv>
      <pdo6ma>0</pdo6ma>
      <pdo6mv>0</pdo6mv>
      <pdo7ma>0</pdo7ma>
      <pdo7mv>0</pdo7mv>
    </BM_PDO_Sink>
    <BM_PDO_Source>
      <pdo1ma>3000</pdo1ma>
      <pdo1mv>5000</pdo1mv>
      <pdo2ma>3000</pdo2ma>
      <pdo2mv>9000</pdo2mv>
      <pdo3ma>0</pdo3ma>
      <pdo3mv>0</pdo3mv>
      <pdo4ma>0</pdo4ma>
      <pdo4mv>0</pdo4mv>
      <pdo5ma>0</pdo5ma>
      <pdo5mv>0</pdo5mv>
      <pdo6ma>0</pdo6ma>
      <pdo6mv>0</pdo6mv>
      <pdo7ma>0</pdo7ma>
      <pdo7mv>0</pdo7mv>
    </BM_PDO_Source>
    <BM_PDO_Sink_2>
      <pdo1ma>3000</pdo1ma>
      <pdo1mv>5000</pdo1mv>
      <pdo2ma>0</pdo2ma>
      <pdo2mv>0</pdo2mv>
      <pdo3ma>0</pdo3ma>
      <pdo3mv>0</pdo3mv>
      <pdo4ma>0</pdo4ma>
      <pdo4mv>0</pdo4mv>
      <pdo5ma>0</pdo5ma>
      <pdo5mv>0</pdo5mv>
      <pdo6ma>0</pdo6ma>
      <pdo6mv>0</pdo6mv>
      <pdo7ma>0</pdo7ma>
      <pdo7mv>0</pdo7mv>
    </BM_PDO_Sink_2>
  </PDO_Configuration>
  <Timer>
    <srt>0</srt>
    <hrt>0</hrt>
    <sct>0</sct>
    <dit>0</dit>
    <srcrt>0</srcrt>
    <trt>0</trt>
    <sofft>0</sofft>
    <nrt>0</nrt>
    <swct>0</swct>
    <snkrt>0</snkrt>
    <dt>0</dt>
    <cnst>0</cnst>
  </Timer>
```


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```
    <Control>
      <i2caddr>0</i2caddr>
      <prou>0</prou>
      <trim1>0</trim1>
      <trim2>0</trim2>
      <extdc>true</extdc>
    </Control>
  </Power_Delivery>
```


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Appendix B – PassThrough.xml


```
<Power_Delivery>
    <Configuration>
      <srprs>true</srprs>
      <srapprs>true</srapprs>
      <srrprs>false</srrprs>
      <saprs>false</saprs>
      <vconns>false</vconns>
      <passthru>true</passthru>
      <extmcu>false</extmcu>
      <pd2en>true</pd2en>
      <pd1autoclk>false</pd1autoclk>
      <pd2autoclk>false</pd2autoclk>
      <useefuse>true</useefuse>
      <extvconn>false</extvconn>
    </Configuration>
    <GPIO_Configuration>
      <count>3</count>
      <gpio1>4</gpio1>
      <gpio2>0</gpio2>
      <gpio3>3</gpio3>
      <gpio4>N/A</gpio4>
      <gpio5>N/A</gpio5>
      <gpio6>N/A</gpio6>
      <gpio7>N/A</gpio7>
      <pd1lden>2</pd1lden>
      <pd2lden>N/A</pd2lden>
      <dispin>5</dispin>
      <disenbm>Drive Hi</disenbm>
      <disdisbm>Drive Low</disdisbm>
      <ccselect>N/A</ccselect>
    </GPIO_Configuration>
    <ISET_Configuration>
      <iset1>6</iset1>
      <iset2>6</iset2>
      <iset3>6</iset3>
      <extiset>false</extiset>
      <isetpd2>false</isetpd2>
      <iseten>true</iseten>
    </ISET_Configuration>
    <BM_Configuration>
      <GPIO_BM_PDO1>
        <GPIO1>Drive Hi</GPIO1>
        <GPIO2>Drive Low</GPIO2>
        <GPIO3>Drive Hi</GPIO3>
        <GPIO4>Don't Care</GPIO4>
        <GPIO5>Don't Care</GPIO5>
        <GPIO6>Don't Care</GPIO6>
        <GPIO7>Don't Care</GPIO7>
      </GPIO_BM_PDO1>
      <GPIO_BM_PDO2>
        <GPIO1>Drive Hi</GPIO1>
        <GPIO2>Drive Low</GPIO2>
        <GPIO3>Drive Hi</GPIO3>
        <GPIO4>Don't Care</GPIO4>
        <GPIO5>Don't Care</GPIO5>
        <GPIO6>Don't Care</GPIO6>
        <GPIO7>Don't Care</GPIO7>
      </GPIO_BM_PDO2>
      <GPIO_BM_PDO3>
        <GPIO1>Drive Hi</GPIO1>
```


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```
        <GPIO2>Drive Low</GPIO2>
        <GPIO3>Drive Hi</GPIO3>
        <GPIO4>Don't Care</GPIO4>
        <GPIO5>Don't Care</GPIO5>
        <GPIO6>Don't Care</GPIO6>
        <GPIO7>Don't Care</GPIO7>
      </GPIO_BM_PDO3>
      <GPIO_BM_PDO4>
        <GPIO1>Drive Hi</GPIO1>
        <GPIO2>Drive Low</GPIO2>
        <GPIO3>Drive Hi</GPIO3>
        <GPIO4>Don't Care</GPIO4>
        <GPIO5>Don't Care</GPIO5>
        <GPIO6>Don't Care</GPIO6>
        <GPIO7>Don't Care</GPIO7>
      </GPIO_BM_PDO4>
      <GPIO_BM_PDO5>
        <GPIO1>Drive Hi</GPIO1>
        <GPIO2>Drive Low</GPIO2>
        <GPIO3>Drive Hi</GPIO3>
        <GPIO4>Don't Care</GPIO4>
        <GPIO5>Don't Care</GPIO5>
        <GPIO6>Don't Care</GPIO6>
        <GPIO7>Don't Care</GPIO7>
      </GPIO_BM_PDO5>
      <GPIO_BM_PDO6>
        <GPIO1>Drive Hi</GPIO1>
        <GPIO2>Drive Low</GPIO2>
        <GPIO3>Drive Hi</GPIO3>
        <GPIO4>Don't Care</GPIO4>
        <GPIO5>Don't Care</GPIO5>
        <GPIO6>Don't Care</GPIO6>
        <GPIO7>Don't Care</GPIO7>
      </GPIO_BM_PDO6>
      <GPIO_BM_PDO7>
        <GPIO1>Drive Hi</GPIO1>
        <GPIO2>Drive Low</GPIO2>
        <GPIO3>Drive Hi</GPIO3>
        <GPIO4>Don't Care</GPIO4>
        <GPIO5>Don't Care</GPIO5>
        <GPIO6>Don't Care</GPIO6>
        <GPIO7>Don't Care</GPIO7>
      </GPIO_BM_PDO7>
      <VSET0V>
        <GPIO1>Drive Low</GPIO1>
        <GPIO2>Drive Low</GPIO2>
        <GPIO3>Drive Low</GPIO3>
        <GPIO4>Don't Care</GPIO4>
        <GPIO5>Don't Care</GPIO5>
        <GPIO6>Don't Care</GPIO6>
        <GPIO7>Input Mode</GPIO7>
      </VSET0V>
      <VSAFE5V>
        <GPIO1>Drive Low</GPIO1>
        <GPIO2>Drive Low</GPIO2>
        <GPIO3>Drive Low</GPIO3>
        <GPIO4>Drive Low</GPIO4>
        <GPIO5>Drive Low</GPIO5>
        <GPIO6>Drive Low</GPIO6>
        <GPIO7>Drive Low</GPIO7>
      </VSAFE5V>
    </BM_Configuration>
    <PDO_Configuration>
```


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```
    <BM_PDO_Sink>
      <pdo1ma>3000</pdo1ma>
      <pdo1mv>5000</pdo1mv>
      <pdo2ma>0</pdo2ma>
      <pdo2mv>0</pdo2mv>
      <pdo3ma>0</pdo3ma>
      <pdo3mv>0</pdo3mv>
      <pdo4ma>0</pdo4ma>
      <pdo4mv>0</pdo4mv>
      <pdo5ma>0</pdo5ma>
      <pdo5mv>0</pdo5mv>
      <pdo6ma>0</pdo6ma>
      <pdo6mv>0</pdo6mv>
      <pdo7ma>0</pdo7ma>
      <pdo7mv>0</pdo7mv>
    </BM_PDO_Sink>
    <BM_PDO_Source>
      <pdo1ma>3000</pdo1ma>
      <pdo1mv>5000</pdo1mv>
      <pdo2ma>0</pdo2ma>
      <pdo2mv>0</pdo2mv>
      <pdo3ma>0</pdo3ma>
      <pdo3mv>0</pdo3mv>
      <pdo4ma>0</pdo4ma>
      <pdo4mv>0</pdo4mv>
      <pdo5ma>0</pdo5ma>
      <pdo5mv>0</pdo5mv>
      <pdo6ma>0</pdo6ma>
      <pdo6mv>0</pdo6mv>
      <pdo7ma>0</pdo7ma>
      <pdo7mv>0</pdo7mv>
    </BM_PDO_Source>
    <BM_PDO_Sink_2>
      <pdo1ma>3000</pdo1ma>
      <pdo1mv>5000</pdo1mv>
      <pdo2ma>0</pdo2ma>
      <pdo2mv>0</pdo2mv>
      <pdo3ma>0</pdo3ma>
      <pdo3mv>0</pdo3mv>
      <pdo4ma>0</pdo4ma>
      <pdo4mv>0</pdo4mv>
      <pdo5ma>0</pdo5ma>
      <pdo5mv>0</pdo5mv>
      <pdo6ma>0</pdo6ma>
      <pdo6mv>0</pdo6mv>
      <pdo7ma>0</pdo7ma>
      <pdo7mv>0</pdo7mv>
    </BM_PDO_Sink_2>
  </PDO_Configuration>
  <Timer>
    <srt>27</srt>
    <hrt>30</hrt>
    <sct>190</sct>
    <dit>45</dit>
    <srcrt>750</srcrt>
    <trt>500</trt>
    <sofft>890</sofft>
    <nrt>4000</nrt>
    <swct>320</swct>
    <snkrt>110</snkrt>
    <dt>100</dt>
    <cnst>40</cnst>
  </Timer>
```


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```
    <Control>
      <i2caddr>20</i2caddr>
      <prou>0</prou>
      <trim1>0</trim1>
      <trim2>0</trim2>
      <extdc>false</extdc>
    </Control>
  </Power_Delivery>
```


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Appendix C – References

Document References

Application and Technical Notes

AN_175 Battery Charger Detection over USB with FT-X Devices

TN_181 Type-C USB Connectors with FTDI Products

AN_551 FT4232HP FT2232HP FT232HP Configuration Guide

AN_449 FT4233HP FT2233HP FT233HP FT4232HP FT2232HP FT232HP DCDC Power Delivery Application Note

USB 2.0 High Speed (with PD) References

FTDI USB High Speed ICs with PD Support

USB 2.0 High Speed (no PD) References

FTDI USB High Speed ICs

FTDI USB Full Speed ICs

SuperSpeed References

FTDI SuperSpeed ICs

FTDI SuperSpeed Modules

HD3SS3220 Type-C mux

TIDA-00891 USB Type-C Plug to USB Type-A Receptacle SuperSpeed MUX With UFP Controller Reference Design

USB High Speed Modules

FT_PROG

Acronyms and Abbreviations

Terms	Description
CC	Configuration Channel
EEPROM	Electrically Erasable Programmable Read Only Memory
FIFO	First In First Out
JTAG	Joint Test Action Group
I2C	Inter-Integrated Circuit
ICs	Integrated Circuits

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Terms	Description
MPSSE	Multi-Protocol Synchronous Serial Engine
PD	Power Delivery
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus

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Appendix D – List of Tables and Figures

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Appendix E – Revision History

Document Title: TN_185 What is USB Power Delivery?
Document Reference No.: FT_001559
Clearance No.: FTDI#588
Product Page: https://ftdichip.com/product-category/products/ic/
Document Feedback: Send Feedback

Revision	Changes	Date
1.0	Initial Release	21-11-2023

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