

# **Technical Notes**

**TN\_161** 

## FT4222H Errata Technical Note

#### Version 1.6

Issue Date: 12-10-2023

The intention of this errata technical note is to give a detailed description of known functional or electrical issues with the FTDI FT4222H series device.

The current revision of the FT4222H series is **Revision D, released April 2018.** 

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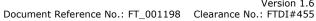


#### Technical Note TN\_161 FT4222H Errata Technical Note

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## 1 FT4222H Revision

FT4222H part numbers are listed in Table 1-1. The letter at the end of the date code identifies the device revision.

The current revision of the FT4222H series is Revision D, released April 2018.

Part Number	Package
FT4222HQ	32 pin VQFN

Table 1-1 FT4222H Part Numbers

These errata technical note covers the revisions of FT4222H listed in Table 1-2.

Revision	Notes					
Α	A First device revision. Launched Sep 2014					
B Second device revision. Launched Sep 2015						
C Third device revision. Launched Oct 2016						
D	Forth device revision. Launched Apr 2018					

Table 1-2 FT4222H Series Revisions



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# 2 Errata History Table – Functional Errata

Functional Errata	Short description	Errata occurs in device revision		
FT4222H	Android issues	Α		
FT4222H	CPU usage too high	А		
FT4222H	I <sup>2</sup> C combined message support	А		
FT4222H	Default pin status change	Α		
FT4222H	More suspend setting support	Α		
FT4222H	Custom PID settings are ignored	В		
FT4222H	Slow response after the host restarts	В		
FT4222H	SPI master in single mode	В		
FT4222H	I2C Data path is not fully reset	A, B, C		
FT4222H	Not Response STALL to Get BOS Descriptor defined in USB3.0	А, В, С		
FT4222H	Flash operation mode support	A, B, C		
FT4222H	SPI slave data lost	A, B, C		
FT4222H				
FT4222H	Error handling: writes over the range of the data buffer	A, B, C, D		

**Table 2-1 Functional Errata** 

# 2.1 Errata History Table – Electrical and Timing Specification Deviations

Deviations	Short description	Errata occurs in device revision
-	No known issues	-

**Table 2-2 Electrical and Timing Errata** 

#### 3 Functional Errata of FT4222H

#### 3.1 Revision A

#### 3.1.1 Android issues

#### **Introduction:**

FT4222H supports Android devices. With J2XX, it is possible to develop an app utilizing the FT4222H.

#### Issue:

The following issues may happen when the FT4222H connects to an Android device.

- 1. The FT4222H works as an SPI master, it may reset during transferring data.
- 2. The FT4222H works as I<sup>2</sup>C slave, the last byte may be lost when the receiving buffer is full.

#### Workaround:

There are no known workarounds available. This issue is corrected at Revision B.

#### Package specific:

The effected packages are listed in Table 3-1.

Package	Applicable (Yes/No)
FT4222HQ	Yes

**Table 3-1 Affected Packages** 

#### 3.1.2 CPU usage and latency timer issue

#### Introduction:

In USB, data is received from the device to the PC by a polling method. The driver will request a certain amount of data from the USB scheduler. The latency timer is provided to allow efficient polling and flushing short data packets.

#### **Issue:**

The FT4222H does not support the latency timer feature and causes the USB scheduler to be busy and uses too much CPU resource.

#### **Workaround:**

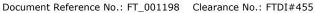
There are no known workarounds available. This issue is corrected at Revision B.

#### Package specific:

The effected packages are listed in Table 3-2.

Package	Applicable (Yes/No)
FT4222HQ	Yes

**Table 3-2 Affected Packages** 





### 3.1.3 I<sup>2</sup>C combined message issue

#### **Introduction:**

A master issue at least two reads and/or writes to one or more slaves. In a combined message, each read or write begins with a START and the slave address. After the first START, the subsequent starts are referred to as repeated START bits; repeated START bits are not preceded by STOP bits, which indicate to the slave the next transfer is part of the same message.

Start		Write	ACK	8-bit data		SR	7-bit slave address	Read	ACK	8-bit data	ACK	8-bit data	S	STOP	
-------	--	-------	-----	------------	--	----	---------------------	------	-----	------------	-----	------------	---	------	--

#### **Issue:**

Some  $I^2C$  devices need to communicate with a combined message format. However, the FT4222H does not support this feature.

#### Workaround:

There are no known workarounds available. The feature of  $I^2C$  combined messages will be supported at Revision B.

#### Package specific:

The effected packages are listed in Table 3-3.

Package	Applicable (Yes/No)
FT4222HQ	Yes

**Table 3-3 Affected Packages** 

#### 3.1.4 Default pin status

#### **Introduction:**

By default, the FT4222H will be initialized as an SPI master after power on. When the FT4222H is ready, i.e., finishes USB enumeration, the status of the pins of the Revision A device is as shown in Table 3-4:

Pin num	Pin name	Mode 0	Mode 1	Mode 2	Mode 3
8	SCK	SCK (OUT, low)	SCK (OUT, low)	SCK (OUT, low)	SCK (OUT, low)
9	MISO	MISO (IN)	MISO (IN)	MISO (IN)	MISO (IN)
10	MOSI	MOSI (OUT, high)	MOSI (OUT, high)	MOSI (OUT, high)	MOSI (OUT, high)
11	IO2	IO2 (IN)	IO2 (IN)	IO2 (IN)	IO2 (IN)
12	IO3	IO3 (IN)	IO3 (IN)	IO3 (IN)	IO3 (IN)
13	GPIO0	GPIO0 (OUT, low)	SS10 (OUT, low)	SS10 (OUT, low)	GPIO0 (OUT, low)
14	GPIO1	GPIO1 (OUT, low)	SS20 (OUT, low)	SS20 (OUT, low)	GPIO1 (OUT, low)
15	GPIO2	suspend out (OUT, low)	suspend out (OUT, low)	SS30 (OUT, low)	suspend out (OUT, low)
16	GPIO3	remote wakeup (IN)	remote wakeup (IN)	remote wakeup (IN)	remote wakeup (IN)
17	SS00	SS00 (OUT, low)	SS00 (OUT, low)	SS00 (OUT, low)	SS00 (OUT, low)

Pin num	Pin name	Mode 0	Mode 1	Mode 2	Mode 3
32	SS	SS (IN)	SS (IN)	SS (IN)	SS (IN)

Table 3-4 Revision A FT4222H ready

In the Revision B, the pin status will be changed as per Table 3-5 below:

Pin num	Pin name	Mode 0	Mode 1	Mode 2	Mode 3
8	SCK	SCK (OUT, low)	SCK (OUT, low)	SCK (OUT, low)	SCK (OUT, low)
9	MISO	MISO (IN)	MISO (IN)	MISO (IN)	MISO (IN)
10	MOSI	MOSI (OUT, high)	MOSI (OUT, high)	MOSI (OUT, high)	MOSI (OUT, high)
11	IO2	IO2 (IN)	IO2 (IN)	IO2 (IN)	IO2 (IN)
12	IO3	IO3 (IN)	IO3 (IN)	IO3 (IN)	IO3 (IN)
13	GPIO0	GPIO0 (IN)	SS10 (OUT, high)	SS10 (OUT, high)	GPIO0 (IN)
14	GPIO1	GPIO1 (IN)	SS20 (OUT, high)	SS20 (OUT, high)	GPIO1 (IN)
15	GPIO2	suspend out (OUT, low)	suspend out (OUT, low)	SS30 (OUT, high)	suspend out (OUT, low)
16	GPIO3	remote wakeup (IN)	remote wakeup (IN)	remote wakeup (IN)	remote wakeup (IN)
17	SS00	SS00 (OUT, high)	SS00 (OUT, high)	SS00 (OUT, high)	SS00 (OUT, high)
32	SS	SS (IN)	SS (IN)	SS (IN)	SS (IN)

Table 3-5 Revision B FT4222H ready

#### Package specific:

The effected packages are listed in Table 3-6.

Package	Applicable (Yes/No)
FT4222HQ	Yes

**Table 3-6 Affected Packages** 

#### 3.1.5 Additional Suspend Settings Supported

#### **Introduction:**

The FT4222H provides flexible settings for suspend behavior via FT\_Prog. The Revision B of the FT4222H device provides additional options for customers to configure the pin status during suspend.

- SUSPEND\_OUT\_POL
  - Suspend output is High active. (default)
  - Suspend output is Low active.
- SPI SUSPEND MODE
  - o Disable SPI IP and make SPI pins input (tri-state). (default)
  - Keep SPI pin status when the FT4222H suspends.
  - Enable SPI pin control. Refer to SPI\_SUSPEND for detail settings.
- SPI\_SUSPEND (enable by SPI\_SUSPEND\_MODE)
  - miso\_suspend
    - push low when suspend
    - push high when suspend
  - mosi\_suspend
    - push low when suspend
    - push high when suspend

- io2\_io3\_suspend
  - push low when suspend
  - push high when suspend
- o ss00\_suspend
  - No change (default)
  - push low when suspend
  - push high when suspend
- GPIO\_SUSPEND
  - o gpio0\_suspend
    - No change (default)
    - input (tri-state)
    - push low when suspend
    - push high when suspend
  - o gpio1\_suspend
    - No change (default)
    - input (tri-state)
    - push low when suspend
    - push high when suspend
  - o gpio2\_suspend
    - No change (default)
    - input (tri-state)
    - push low when suspend
    - push high when suspend
  - o gpio3\_suspend
    - No change (default)
    - input (tri-state)
    - push low when suspend
    - push high when suspend

The default pin status of the Revision A device during suspend is shown in Table 3-7.

Pin num	Pin name	Mode 0	Mode 1	Mode 2	Mode 3
8	SCK	SCK (OUT, low)	SCK (OUT, low)	SCK (OUT, low)	SCK (OUT, low)
9	MISO	MISO (OUT, low)	MISO (OUT, low)	MISO (OUT, low)	MISO (OUT, low)
10	MOSI	MOSI (OUT, low)	MOSI (OUT, low)	MOSI (OUT, low)	MOSI (OUT, low)
11	IO2	IO2 (OUT, low)	IO2 (OUT, low)	IO2 (OUT, low)	IO2 (OUT, low)
12	IO3	IO3 (OUT, low)	IO3 (OUT, low)	IO3 (OUT, low)	IO3 (OUT, low)
13	GPIO0	GPIO0 (OUT, low)	SS10 (OUT, no change)	SS10 (OUT, no change)	GPIO0 (OUT, low)
14	GPIO1	GPIO1 (OUT, low)	SS20 (OUT, no change)	SS20 (OUT, no change)	GPIO1 (OUT, low)
15	GPIO2	suspend out (OUT, high)	suspend out (OUT, high)	SS30 (OUT, no change)	suspend out (OUT, high)
16	GPIO3	remote wakeup (IN)	remote wakeup (IN)	remote wakeup (IN)	remote wakeup (IN)
17	SS00	SS00 (OUT, no change)	SS00 (OUT, no change)	SS00 (OUT, no change)	SS00 (OUT, no change)
32	SS	SS (IN)	SS (IN)	SS (IN)	SS (IN)

Table 3-7 Revision A FT4222H suspend



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In the Revision B device, the default suspend setting is changed as per Table 3-8 below:

Pin num	Pin name	Mode 0	Mode 1	Mode 2	Mode 3
8	SCK	SCK (tri-state)	SCK (tri-state)	SCK (tri-state)	SCK (tri-state)
9	MISO	MISO (IN)	MISO (IN)	MISO (IN)	MISO (IN)
10	MOSI	MOSI (IN)	MOSI (IN)	MOSI (IN)	MOSI (IN)
11	IO2	IO2 (IN)	IO2 (IN)	IO2 (IN)	IO2 (IN)
12	IO3	IO3 (IN)	IO3 (IN)	IO3 (IN)	IO3 (IN)
13	GPIO0	GPIO0 (no change)	SS10 (OUT, no change)	SS10 (OUT, no change)	GPIO0 (no change)
14	GPIO1	GPIO1 (no change)	SS20 (OUT, no change)	SS20 (OUT, no change)	GPIO1 (no change)
15	GPIO2	suspend out (OUT, high)	suspend out (OUT, high)	SS30 (OUT, no change)	suspend out (OUT, high)
16	GPIO3	remote wakeup (IN)	remote wakeup (IN)	remote wakeup (IN)	remote wakeup (IN)
17	SS00	SS00 (OUT, no change)	SS00 (OUT, no change)	SS00 (OUT, no change)	SS00 (OUT, no change)
32	SS	SS (IN)	SS (IN)	SS (IN)	SS (IN)

Table 3-8 Revision B FT4222H suspend

#### Package specific:

The effected packages are listed in Table 3-9.

Package	Applicable (Yes/No)
FT4222HQ	Yes

**Table 3-9 Affected Packages** 

#### 3.2 Revision B

#### 3.2.1 Custom PID Settings are ignored

#### Introduction:

It is not possible to change the PID on the FT4222H from our default value of 601C to a custom value. Note, there are no problems changing the VID.

#### Issue:

Any changes made to the PID using the OTP are ignored and the value returns to its default state.

#### **Workaround:**

There are no known workarounds available. This issue is corrected at Revision C.

#### Package specific:

The effected packages are listed in Table 3-10.

Package	Applicable (Yes/No)
FT4222HQ	Yes

**Table 3-10 Affected Packages** 



#### 3.2.2 Slow Response after the Host Restarts

#### **Issue:**

After the host restarts, the FT4222H may have slow response or output unexpected bytes from its USB interface.

#### Workaround:

There are no known workarounds available. This issue is corrected at Revision C.

#### Package specific:

The effected packages are listed in Table 3-11.

Package	Applicable (Yes/No)
FT4222HQ	Yes

Table 3-11 Affected Packages

#### 3.2.3 SPI master in single mode loses data and no response

#### Issue:

The SPI master in single mode may lose the last byte and then no response. This issue may be observed easily in the following configurations:

- 48M/128, 48M/256, 48M/512
- 24M/64, 24M/128, 24M/256, 24M/512

When this issue happens, the support lib function FT4222\_SPIMaster\_SingleReadWrite may not return, or return FT\_FAILED\_TO\_WRITE\_DEVICE.

This issue can be observed with the Revision A also.

#### **Workaround:**

There are no known workarounds available. This issue is corrected at revision C.

#### Package specific:

The effected packages are listed in Table 3-12.

Package	Applicable (Yes/No)
FT4222HQ	Yes

**Table 3-12 Affected Packages** 





#### 3.3 Revision C

#### 3.3.1 Data path is not fully reset when a reset on I<sup>2</sup>C is executed

#### Issue:

When the  $I^2C$  bus encounters errors or works abnormally, users can use the reset APIs to reset the  $I^2C$  function. When a reset command is received, only the  $I^2C$  controller is reset. The transferring data may still be left in the related USB pipe. The USB pipe associated to  $I^2C$  functions should also be reset as the initial status for the next transfer.

#### Workaround:

There are no known workarounds available. This issue is corrected at Revision D.

#### Package specific:

The effected packages are listed in Table 3-13.

Package	Applicable (Yes/No)
FT4222HQ	Yes

**Table 3-13 Effected Packages** 

#### 3.3.2 No Response STALL to Get BOS Descriptor defined in USB3.0

#### Issue:

BOS (Binary device Object Store) descriptor is a newly defined descriptor in the USB3.0 specification. Since the FT4222H is a USB2.0 compliant USB device, getting a BOS descriptor command is not supported. A STALL should be returned, but the FT4222H returns NAKs.

#### Workaround:

There are no known workarounds available. This issue is corrected at Revision D.

#### Package specific:

The affected packages are listed in Table 3-14.

Package	Applicable (Yes/No)
FT4222HQ	Yes

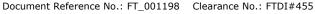
**Table 3-14 Affected Packages** 

#### 3.3.3 Flash Operating Mode Support

#### **Issue:**

When accessing Toshiba flash with SPI Master Quad mode, FT4222H will hang without giving any responses.

FT4222H operates as master with supporting Dual or Quad SPI with three phases as illustrated in **Figure 3.1**.



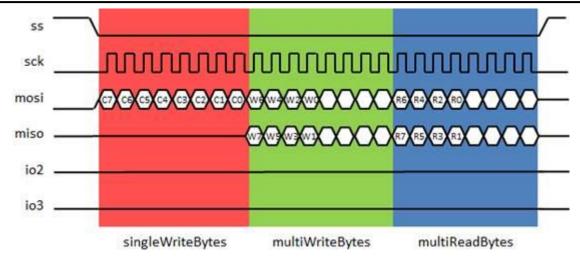


Figure 3.1 Quad SPI with Multi Write Phase

As shown in **Figure 3.1**, 'C', 'W' and 'R', correspond to "Command Phase", "Write Phase" and "Read Phase", where there are information/data in all three phases that are to be exchanged.

Some flash devices operate with single write and multi read protocol but without the multi write phase as illustrated in **Figure 3.2**:

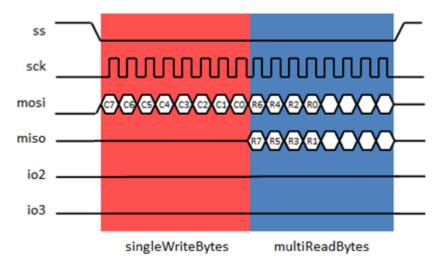


Figure 3.2 Quad SPI without Multi Write Phase

Write Phase has no information/data to transfer. This combination of operating mode is not supported with Revision A, B, and C.

#### Workaround:

In SPI Master Quad mode, the operation of single write with quad read was not supported. No workaround was provided, this feature is implemented with Revision D.

#### Package specific:

The affected packages are listed in Table 3-15.

Package	Applicable (Yes/No)
FT4222HQ	Yes

**Table 3-15 Affected Packages** 

#### 3.3.4 SPI Slave Data Lost

#### Issue:

When operating in SPI Slave mode, the FT4222H would occasionally lose data packets.

#### Workaround:

Verified that the latency Timer configuration was not correct, hence causing no full packet responses, instead all packets responded with short packets. This results in packet drops with D2XX driver. No workaround was provided, this issue is corrected at Revision D.

#### Package specific:

The effected packages are listed in Table 3-16.

Package	Applicable (Yes/No)
FT4222HQ	Yes

**Table 3-16 Affected Packages** 

#### 3.4 Revision D

#### 3.4.1 SPI Slave may lose data when transfer frequency is set to 20MHz

#### Issue:

When operating in SPI Slave mode and receiving large data (>10Kbytes), data loss may occur if the transfer frequency is 20MHz.

#### Workaround:

Downgrade the transfer frequency to 5MHz.

#### Package specific:

The effected packages are listed in Table 3-17.

Package	Applicable (Yes/No)	
FT4222HQ	Yes	

Table 3-17 Affected Packages

# 3.4.2 I<sup>2</sup>C data is corrupt when FT4222\_I2CMaster\_GetStatus is being called

#### Issue:

An error would happen when  $I^2C$  master is writing data and FT4222\_I2CMaster\_GetStatus is being called at the same time.

#### Workaround:

Call FT4222\_I2CMaster\_GetStatus after the end of I<sup>2</sup>C transmission.

#### Package specific:

The effected packages are listed in Table 3-188.

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Package	Applicable (Yes/No)	
FT4222HQ	Yes	

**Table 3-18 Affected Packages** 

#### 3.5 Bus Error condition in USB Device Controller

# 3.5.1 The USB Device Controller writes past the range of the data buffer when a babble error occurs

#### **Introduction:**

A babble error occurs when USB device receives more data than the maximum packet size.

#### Issue:

If the data packet comes with the correct CRC16, the USB Device Controller accepts it and responds with ACK. It then writes the data over the address boundary of the data buffer for the endpoint.

If the data packet comes with the incorrect CRC16, the USB Device Controller discards it and times out. However, it still writes the data over the address boundary of the data buffer for the endpoint.

#### Workaround:

Currently, there is no workaround for this issue.

#### Package specific:

The effected packages are listed in Table 3-199.

Package	Applicable (Yes/No)	
FT4222HQ	Yes	

**Table 3-19 Affected Packages** 

## 3.6 MISO send data at wrong timing in SPI Slave Mode

#### 3.6.1 MISO change the data polarity at wrong timing

#### Introduction:

The data output of FT4222 in SPI slave mode does not comply with the well-known SPI spec. MISO change the data polarity at wrong timing.

#### Issue:

The SPI spec defines CPHA and CPOL to configure the clock polarity and phase with respect to the data. CPHA decides when MISO pin changes the IO polarity.

Take CPHA = 0 as example.

The SPI SPEC describe:

- 1. The first data bit is outputted immediately when CS activates.
- 2. The MISO changes IO polarity on trailing phase to make sure the data can be got the correct data on leading phase.

The issue happens on item 2.

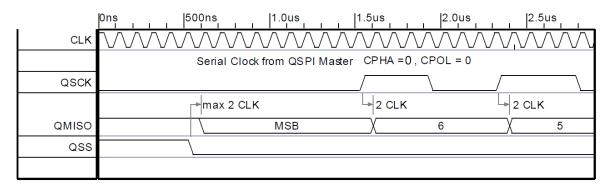
As shown in the diagram below, FT4222 changes the IO polarity after 2 CLK (25ns) after leading phase happens. This issue may not cause problem when SPI Master is a hardware decode IP. However, if the SPI Master is a MCU base design with low sampling rate, the master might retrieve the wrong data.

#### Workaround:

Currently, there is no workaround for this issue. When leading phase happens, the SPI master needs to retrieve data as soon as possible. If the process cannot finish in 25ns, the data will be overwritten by the next data bit.

#### Package specific:

The effected packages are listed in Table 3-20.



Note: 2CLK = 25ns

Package	Applicable (Yes/No)	
FT4222HQ	Yes	

**Table 3-20 Affected Packages** 



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## 4 FT4222H Series Package Markings

The FT4222H is supplied in a RoHS compliant leadless VQFN-32 package. The package is lead (Pb) free and uses a 'green' compound. The package is fully compliant with European Union directive 2002/95/EC. An example of the markings on the package is shown in Figure 4.1 below.

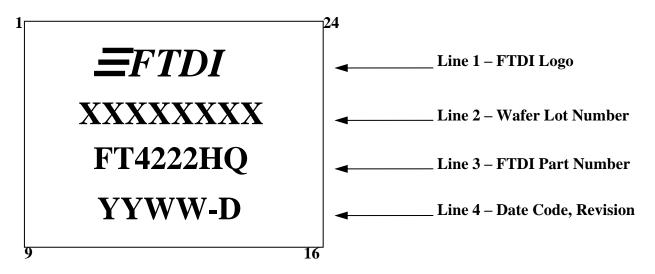


Figure 4.1 VQFN-32 Package Markings

The date code format is YYWW where WW = 2-digit week number, YY = 2-digit year number. This is followed by the revision number.

The code **XXXXXXXX** is the manufacturing LOT code.



### TN\_161 FT4222H Errata Technical Note

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# **Appendix A - References**

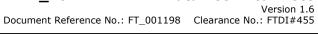
## **Document References**

NA

## **Acronyms and Abbreviations**

Terms	Description
CPU	Central Processing Unit
GPIO	General Purpose Input/output
I2C	Inter-Integrated Circuit
MISO	Master In Slave Out
MOSI	Master Out Slave In
PC	Personal Computer
SS	Slave Select
SCK	Serial Clock
SPI	Serial Peripheral Interface
USB	Universal Serial Bus
VQFN	Very Thin Quad Flat Non-Leaded Package







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**TN\_161 FT4222H Errata Technical Note**Version 1.6

Document Reference No.: FT\_001198 Clearance No.: FTDI#455

# **Appendix C - Revision History**

Document Title: TN\_161 FT4222H Errata Technical Note

Document Reference No.: FT\_001198
Clearance No.: FTDI# 455

Product Page: <a href="http://www.ftdichip.com/Products/ICs/FT4222H.html">http://www.ftdichip.com/Products/ICs/FT4222H.html</a>

Document Feedback: Send Feedback

Revision	Changes	Date
1.0	Initial Release	31-08-2015
1.1	Updated with custom PID issue.	17-05-2016
1.2	Updated with rev C fixes	18-10-2016
1.3	Updated with rev D fixes	28-03-2018
1.4	Updated for IO_ERROR occurs	15-04-2020
1.5	Updated for Section 3.4.1	21-03-2022
1.6	Added section 3.6	12-10-2023