The intention of this technical note is to give a detailed description of improvement of the FT4222H Revision C device. The current revision of the FT4222H series is Revision C, released Sep 2016.
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1 Introduction

The FT4222H is a Hi-Speed USB interface device which supports SPI and I2C communication protocol with configurable interfaces. The SPI interface can be configured in master mode with single, dual, or quad bits data width transfer or in slave mode with single bit data width transfer.

The rev C of the FT4222H largely improves SPI master throughput.

1.1 SPI master performance improvement

The FT4222H SPI master throughput is improved at revision C. For example, the throughput of SPI quad write is improved from 28.1Mbps to 53.8Mbps at 80MHz operation clock and 1/2 clock ratio.

<table>
<thead>
<tr>
<th>SCK Freq. (Hz)</th>
<th>SCK = Operating Clock * the following ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1/2</td>
</tr>
<tr>
<td>Operating Clock</td>
<td>Max Throughput can be expected</td>
</tr>
<tr>
<td>80MHz</td>
<td>28.1Mbps*</td>
</tr>
<tr>
<td>60MHz</td>
<td>20.5Mbps*</td>
</tr>
<tr>
<td>48MHz</td>
<td>16.3Mbps*</td>
</tr>
<tr>
<td>24MHz</td>
<td>8.0Mbps*</td>
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</table>

Table 1 The rev.B SCK Operating Frequency in SPI Master Mode

<table>
<thead>
<tr>
<th>SCK Freq. (Hz)</th>
<th>SCK = Operating Clock * the following ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1/2</td>
</tr>
<tr>
<td>Operating Clock</td>
<td>Max Throughput can be expected</td>
</tr>
<tr>
<td>80MHz</td>
<td>53.8Mbps*</td>
</tr>
<tr>
<td>60MHz</td>
<td>39.7Mbps*</td>
</tr>
<tr>
<td>48MHz</td>
<td>31.5Mbps*</td>
</tr>
<tr>
<td>24MHz</td>
<td>15.8Mbps*</td>
</tr>
</tbody>
</table>

Table 2 The rev.C SCK Operating Frequency in SPI Master Mode

*The max. throughput can be expected under the condition of quad mode transfers with a high operating frequency on SCK. It also depends on the USB bus transfer condition. For example, the max throughput that can be expected is up to 28.1Mbps when the operating clock is equal to 80MHz, SCK is set as 20MHz or 40MHz, the data bus is operating in quad mode and the USB bus is operating at hi-speed USB rates with sufficient bandwidth.
2 FT4222H Series Package Markings

The FT4222H is supplied in a RoHS compliant leadless VQFN-32 package. The package is lead (Pb) free, and uses a ‘green’ compound. The package is fully compliant with European Union directive 2002/95/EC. An example of the markings on the package is shown in the figures below.

![Figure 2.1 VQFN-32 Package Markings](image)

The date code format is **YYWW** where **WW** = 2 digit week number, **YY** = 2 digit year number. This is followed by the revision number.

The code **XXXXXXXX** is the manufacturing LOT code.
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Appendix A – References

Document References

DS_FT4222H

Acronyms and Abbreviations

<table>
<thead>
<tr>
<th>Terms</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU</td>
<td>Central Processing Unit</td>
</tr>
<tr>
<td>GPIO</td>
<td>General Purpose Input/output</td>
</tr>
<tr>
<td>I2C</td>
<td>Inter-Integrated Circuit</td>
</tr>
<tr>
<td>MISO</td>
<td>Master In Slave Out</td>
</tr>
<tr>
<td>MOSI</td>
<td>Master Out Slave In</td>
</tr>
<tr>
<td>PC</td>
<td>Personal Computer</td>
</tr>
<tr>
<td>SS</td>
<td>Slave Select</td>
</tr>
<tr>
<td>SCK</td>
<td>Serial Clock</td>
</tr>
<tr>
<td>SPI</td>
<td>Serial Peripheral Interface</td>
</tr>
<tr>
<td>USB</td>
<td>Universal Serial Bus</td>
</tr>
<tr>
<td>VQFN</td>
<td>Very Thin Quad Flat Non-Leaded Package</td>
</tr>
</tbody>
</table>
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## Appendix C – Revision History

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Clearance No.: FTDI# 512  
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Document Feedback: Send Feedback

<table>
<thead>
<tr>
<th>Revision</th>
<th>Changes</th>
<th>Date</th>
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<tbody>
<tr>
<td>1.0</td>
<td>Initial Release</td>
<td>2016-10-05</td>
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