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1 Introduction

The FT60X serial devices are the SuperSpeed USB 3.1 Gen 1 devices of FTDI Chip, the FT600/FT601/FT602 provide USB 3.0 to FIFO Bridge functions. The USB bus speed can be up to 5Gbps. The devices FIFO interfaces have the options of 16 bit (FT600) or 32 bit (F601/FT602) wide parallel FIFO interface. The FT602 is a FIFO to USB3.0 UVC bridge device.

This document explains the main rules of PCB design for the high speed signals of the FT60X devices.

1.1 Overview

The below components and high speed signal traces on the PCB can affect the FT60X device performance.

a. USB 3.0 receptacle and AC coupling on the SuperSpeed TX trace pair
b. SuperSpeed USB traces
c. FIFO bus
d. Clock/crystal circuit
2 PCB design guidelines

2.1 USB3.0 Receptacle

Selecting a USB3.0 receptacle qualified by USB-IF is recommended.

A bad connector may not pass the SuperSpeed USB electrical test and affect the data transfer rate.

2.2 AC Coupling Capacitors on SuperSpeed Signal Trace Pair

TX (TODP and TODN pins) traces only. Place close to the receptacle symmetrically, 0.1uF on each trace is recommended, using a ceramic chip capacitor.

2.3 Number of PCB layers

At least 4 layers are necessary, and 6 layers are recommended.

Table 2.1 and 2.2 show the samples PCB stack up for 4 layers and 6 layers.

<table>
<thead>
<tr>
<th>Layer</th>
<th>Method</th>
</tr>
</thead>
<tbody>
<tr>
<td>Top</td>
<td>Signal</td>
</tr>
<tr>
<td>2nd</td>
<td>GND</td>
</tr>
<tr>
<td>3rd</td>
<td>Power</td>
</tr>
<tr>
<td>Bottom</td>
<td>Signal, GND</td>
</tr>
</tbody>
</table>

Table 2.1 4 Layers PCB Stack up Sample

<table>
<thead>
<tr>
<th>Layer</th>
<th>Method</th>
</tr>
</thead>
<tbody>
<tr>
<td>Top</td>
<td>Signal</td>
</tr>
<tr>
<td>2nd</td>
<td>GND</td>
</tr>
<tr>
<td>3rd</td>
<td>Signal, Power</td>
</tr>
<tr>
<td>4th</td>
<td>Signal, GND</td>
</tr>
<tr>
<td>5th</td>
<td>Power</td>
</tr>
<tr>
<td>Bottom</td>
<td>Signal, GND</td>
</tr>
</tbody>
</table>

Table 2.2 6 Layers PCB Stack up Sample

2.4 SuperSpeed Trace Length

A trace length between the FT60x device and the USB3.0 receptacle of not more than 10 cm (4 inches) on the PCB (FR-4) is recommended.
2.5 Routing of SuperSpeed Traces

Same length, same width, same layer, fixed spacing are key to symmetrical routing for any differential data signal of USB traces including SSTX, SSRX and DP/DN pairs.

No routing layer change for SuperSpeed USB traces (SSTX and SSRX) is recommended. If the routing layer has to be changed, maintain continuous grounding by putting in an appropriate number of vias.

No stub on any SuperSpeed signal trace. Also avoid unexpected stubs.

No need to route symmetrically between different pairs, e.g. SSTX and SSRX.

2.6 Impedance control for USB traces

Signal line impedance of USB is typically 90 Ohms differential. +/-10% accuracy is allowed. Fixed width and fixed spacing between traces in a pair should be maintained to avoid impedance mismatch.

2.7 Routing of FIFO Bus

The FIFO bus operates on a clock that can run up 100MHz. The clock is driven by the FT60x. FIFO bus signals should connect to the FIFO master directly if they are placed on the same PCB as the FT60x device. [Note1]

To ensure signal integrity, same length, same width (>=4mil) traces are recommended for the FIFO bus with signal line impedance set to 50 Ohms single ended, +/-10% accuracy is allowed. [Note2]

Note1: FTDI UMFT60xx module boards connect to FIFO master (FPGA) boards with a high speed connector e.g. HSMC and FMC. The 33 Ohm serial resistors on the FIFO bus are to reduce EMI reflection. A trace length between the FT60x device and the FIFO master of not more than 25.4 cm (10 inches) on the PCB (FR-4) is recommended.

Note 2: As the clock signal is always driven by the FT60x with a frequency higher than the data lines, the delay time of the clock signal should be less than the data lines. Therefore, the trace length of the clock signal should be shorter than the data lines.

2.8 Crystal Requirements and Routing

A general purpose 30 MHz (Frequency=30 MHz, Stability≤±30ppm, ESR≤500hm, Load Capacitance=12~18pF) crystal is recommended.

Place the crystal and the load capacitor on the same layer and near to the FT60x, the signal traces should be shielded by ground.
3 Sample Layout for USB3.0 Micro Receptacle

Figure 3.1 shows a sample layout for the FT60x when using the USB3.0 micro receptacle on the PCB.

![Sample Layout for USB3.0 Micro Receptacle](image)

Figure 3-1 Sample Layout for USB3.0 Micro Receptacle
4 Contact Information

**Head Office – Glasgow, UK**

Future Technology Devices International Limited  
Unit 1, 2 Seaward Place, Centurion Business Park  
Glasgow G41 1HH  
United Kingdom  
Tel: +44 (0) 141 429 2777  
Fax: +44 (0) 141 429 2758  
E-mail (Sales): sales1@ftdichip.com  
E-mail (Support): support1@ftdichip.com  
E-mail (General Enquiries): admin1@ftdichip.com

**Branch Office – Tigard, Oregon, USA**

Future Technology Devices International Limited  
(USA)  
7130 SW Fir Loop  
Tigard, OR 97223-8160  
USA  
Tel: +1 (503) 547 0988  
Fax: +1 (503) 547 0987  
E-Mail (Sales): us.sales@ftdichip.com  
E-Mail (Support): us.support@ftdichip.com  
E-Mail (General Enquiries): us.admin@ftdichip.com

**Branch Office – Taipei, Taiwan**

Future Technology Devices International Limited  
(Taiwan)  
2F, No. 516, Sec. 1, NeiHu Road  
Taipei 114  
Taiwan, R.O.C.  
Tel: +886 (0) 2 8797 1330  
Fax: +886 (0) 2 8751 9737  
E-mail (Sales): tw.sales1@ftdichip.com  
E-mail (Support): tw.support1@ftdichip.com  
E-mail (General Enquiries): tw.admin1@ftdichip.com

**Branch Office – Shanghai, China**

Future Technology Devices International Limited  
(China)  
Room 1103, No. 666 West Huaihai Road,  
Shanghai, 200052  
China  
Tel: +86 21 62351596  
Fax: +86 21 62351595  
E-mail (Sales): cn.sales@ftdichip.com  
E-mail (Support): cn.support@ftdichip.com  
E-mail (General Enquiries): cn.admin@ftdichip.com

**Web Site**

http://ftdichip.com

**Distributor and Sales Representatives**

Please visit the Sales Network page of the [FTDI Web site](http://ftdichip.com) for the contact details of our distributor(s) and sales representative(s) in your country.

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Appendix A – References

Document References
NA

Acronyms and Abbreviations

<table>
<thead>
<tr>
<th>Terms</th>
<th>Description</th>
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<tr>
<td>DN</td>
<td>Data Negative</td>
</tr>
<tr>
<td>DP</td>
<td>Data Positive</td>
</tr>
<tr>
<td>FIFO</td>
<td>First In First Out</td>
</tr>
<tr>
<td>FMC</td>
<td>Field Programmable Mezzanine Card</td>
</tr>
<tr>
<td>HSMC</td>
<td>High Speed Mezzanine Card</td>
</tr>
<tr>
<td>PCB</td>
<td>Print Circuit Board</td>
</tr>
<tr>
<td>SSRX</td>
<td>SuperSpeed Receiver differential pair</td>
</tr>
<tr>
<td>SSTX</td>
<td>SuperSpeed Transceiver differential pair</td>
</tr>
<tr>
<td>USB</td>
<td>Universal Serial Bus</td>
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<thead>
<tr>
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<tr>
<td>1.0</td>
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Document Feedback: [Send Feedback](#)