

Application Note

AN_232R-01

Bit Bang Mode Availability for the FT232R and FT245R

Version 2.03

Issue Date: 2018-07-02

This document describes the 3 Bit Bang Modes available with the FTDI FT232R and FT245R devices. It also gives examples on how to use these 3 modes.

Use of FTDI devices in life support and/or safety applications is entirely at the user's risk, and the user agrees to defend, indemnify and hold FTDI harmless from any and all damages, claims, suits or expense resulting from such use.



Table of Contents

1 Introduction	2
2 Asynchronous Bit Bang Mode	3
3 Synchronous Bit Bang Mode	5
4 CBUS Bit Bang Mode	8
5 Contact Information	9
Appendix A - References	10
Document References	10
Acronyms and Abbreviations	10
Appendix B - List of Tables and Figures	11
List of Tables	11
List of Figures	11
Appendix C - Revision History	12

AN_232R-01 Bit Bang Mode Availability for the FT232R and FT245R Version 2.03



Document No.: FT_000339 Clearance No.: FTDI# 169

1 Introduction

Bit Bang mode is a special <u>FT232R</u> and <u>FT245R</u> device mode that changes the 8 IO lines into an 8 bit bidirectional data bus. There are three types of Bit Bang mode:

- Asynchronous Bit Bang Mode, which is the same as the FTDI BM and C chip-style Bit Bangmode, with the addition of Read and Write strobes in the case of the FT232R.
- Synchronous Bit Bang Mode, where data is only read from the device when the device is written to. This is the same as the FT2232 Synchronous Bit Bang mode.
- CBUS Bit Bang Mode, a new 4-bit version of Bit Bang mode is available on the FT232RCBUS pins.

Asynchronous and Synchronous Bit Bang modes are enabled by driver commands, while CBUS Bit Bang must be set up in the device EEPROM (this can be done using the <u>FT_PROG</u> utility) before it can be enabled with a driver command.

2 Asynchronous Bit Bang Mode

Asynchronous Bit Bang mode is the same as BM-style Bit Bang mode. Any data written to the device in the normal manner will be self-clocked onto the data pins which have been configured as outputs. Each pin can be independently set as an input or an output. The rate that the data is clocked out at is controlled by the Baud rate generator. For the data to change there, has to be new data written and the Baud rate clock has to tick. If no new data is written to the device, the pins will hold the last value written.

When Asynchronous Bit Bang mode is enabled the IO signal lines are configured as follows:

FT232RL/FT245RL Pin Number	FT232RQ/FT245RQ Pin Number	Signal	Туре	Description
1	30	D0	Input/Output	Bit Bang data Bus bit 0
5	2	D1	Input/Output	Bit Bang data Bus bit 1
3	32	D2	Input/Output	Bit Bang data Bus bit 2
11	8	D3	Input/Output	Bit Bang data Bus bit 3
2	31	D4	Input/Output	Bit Bang data Bus bit 4
9	6	D5	Input/Output	Bit Bang data Bus bit 5
10	7	D6	Input/Output	Bit Bang data Bus bit 6
6	3	D7	Input/Output	Bit Bang data Bus bit 7

Table 2.1 Asynchronous Bit Bang Mode IO Configurations

In the case of the FT232R, CBUS0/CBUS1/CBUS2/CBUS3 can be configured to bring out the internal RD# strobe and CBUS0/CBUS1 can be configured to bring out the internal WR# strobe when the device is in Asynchronous Bit Bang mode. This is the same as the Enhanced Asynchronous Bit Bang mode of the FT2232 device. Alternatively, the CBUS pins can be used to provide clock signals by setting the appropriate values in the EEPROM. This can be done using the FT_PROG_utility.

The CBUS must be configured in the FT232R EEPROM. This can be done using the <u>FT_PROG</u> utility. This option is not available for the FT245R.

FT232RL/FT245RL Pin Number	FT232RQ/FT245RQ Pin Number	Signal	Туре	Description
23	22	C0	Input/Output	Configurable function
22	21	C1	Input/Output	Configurable function
13	10	C2	Input/Output	Configurable function
14	11	C3	Input/Output	Configurable function

Table 2.2 CBUS Pins Settings

A number of <u>D2XX driver</u> commands are needed to use Asynchronous Bit Bang mode. The commands of interest are listed below:

D2XX Function	Description
FT_SetBitMode	Asynchronous Bit Bang mode is enabled using the FT_SetBitMode command. A value of 0x01 will enable it and a value of 0x00 will reset the device mode. (see note 1)
FT_SetBaudRate	The rate of data transfer can be controlled by using the FT_SetBaudRate command. The maximum Baud rate is 3MBaud, but to allow time for the data to be setup and held around the WR# strobe the Baud rate should be less than 1MBaud.The clock for the Asynchronous Bit Bang mode is actually 16 times the Baud rate. A value of 9600 Baud would transfer the data at $(9600 \times 16) = 153600$ bytes per second, or 1 every 6.5 μ S.
FT_Write	Data can be written to the device in Asynchronous Bit Bang mode using the FT_Write command. If multiple bytes are written to the device the values on the pins will change at the rate set by FT_SetBaudRate
FT_GetBitMode	FT_GetBitMode returns the instantaneous value of the pins. A single byte will be returned containing the current values of the pins, both those which are inputs and those which are outputs.
FT_Read	FT_Read will return a buffer of values which have been sampled from the pins at the rate set by FT_SetBaudRate. If the read buffers have filled, data will be lost. Each byte returned contains the values of the pins, both those which are inputs and those which are outputs.

Table 2.3 D2XX Commands

Full descriptions of these functions are available in the <u>D2XX Programmer's Guide</u>.

Code examples can be downloaded from Sample Project

Note:

1. FT_SetBitMode command can only enable one mode at a time.



3 Synchronous Bit Bang Mode

Synchronous Bit Bang mode is the same as the FT2232 Synchronous Bit Bang mode. With Synchronous Bit Bang mode, data will only be sent out if there is space in the device for data to be read from the pins. This Synchronous Bit Bang mode will read the data bus pins first, before it sends out the byte that has just been transmitted. It is therefore 1 byte behind the output and so to read the inputs for the byte that you have just sent, another byte must be sent.

For example:

- Pins start at 0xFF
- Send 0x55, 0xAA
- Pins go to 0x55 and then to 0xAA
- Data read = 0xFF, 0x55
- Pins start at 0xFF
- Send 0x55, 0xAA, 0xAA (repeat the last byte sent)
- Pins go to 0x55 and then to 0xAA
- Data read = 0xFF, 0x55, 0xAA

The timing for Synchronous Bit bang is described in this diagram and the table below:

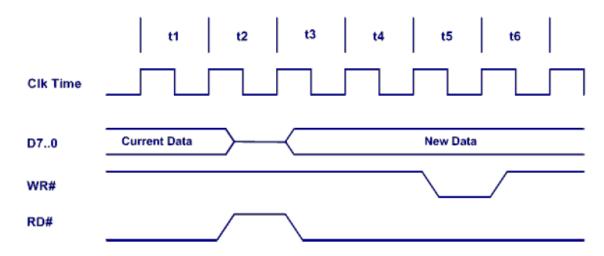


Figure 3.1 Synchronous Bit Bang Timing Diagram

Time	Description
t1	Current pin state is read
t2	RD# is set inactive
t3	RD# is set active again, and any pins that are output will change to the new data.
t4	Clock state for data setup
t5	WR# goes active
t6	WR# goes inactive

Table 3.1 Synchronous Bit Bang Timing

For the data to change there has to be new data written and the Baud rate clock has to tick. If no new data is written to the device, the pins will hold the last value written.



When Synchronous Bit Bang mode is enabled the IO signal lines are configured as follows:

FT232RL/FT245RL Pin Number	FT232RQ/FT245RQ Pin Number	Signal	Туре	Description
1	30	D0	Input/Output	Bit Bang data Bus bit 0
5	2	D1	Input/Output	Bit Bang data Bus bit 1
3	32	D2	Input/Output	Bit Bang data Bus bit 2
11	8	D3	Input/Output	Bit Bang data Bus bit 3
2	31	D4	Input/Output	Bit Bang data Bus bit 4
9	6	D5	Input/Output	Bit Bang data Bus bit 5
10	7	D6	Input/Output	Bit Bang data Bus bit 6
6	3	D7	Input/Output	Bit Bang data Bus bit 7

Table 3.2 Synchronous Bit Bang Mode IO Configurations

In the case of the FT232R, CBUSO/CBUS1/CBUS2/CBUS3 can be configured to bring out the internal RD# strobe and CBUSO/CBUS1 can be configured to bring out the internal WR# strobe when the device is in Synchronous Bit Bang mode. This is the same as the Enhanced Synchronous Bit Bang mode of the FT2232 device. Alternatively, the CBUS pins can be used to provide clock signals by setting the appropriate values in the EEPROM. The CBUS must be configured in the FT232R EEPROM. This can be done using the FT PROG utility. This option is not available for the FT245R.

FT232RL/FT245RL Pin Number	FT232RQ/FT245RQ Pin Number	Signal	Туре	Description
23	22	C0	Input/Output	Configurable function
22	21	C1	Input/Output	Configurable function
13	10	C2	Input/Output	Configurable function
14	11	C3	Input/Output	Configurable function

Table 3.3 EEPROM CBUS Pins Settings

A number of <u>D2XX driver</u> commands are needed to use Synchronous Bit Bang mode. The commands of interest are listed below:

D2XX Function	Description
FT_SetBitMode	Synchronous Bit Bang mode is enabled using the FT_SetBitMode command. A value of 0x04 will enable it and a value of 0x00 will reset the device mode. (please see note 1 in section 2)
FT_SetBaudRate	The rate of data transfer can be controlled by using the FT_SetBaudRate command. The maximum Baud rate is 3MBaud, but to allow time for the data to be setup and held around the WR# strobe the Baud rate should be less than 1MBaud.The clock for the Synchronous Bit Bang mode is actually 16 times the Baud rate. A value of 9600 Baud would transfer the data at $(9600x16) = 153600$ bytes per second, or 1 every 6.5 μ S.
FT_Write	Data can be written to the device in Synchronous Bit Bang mode using the FT_Write command. If multiple bytes are written to the device the values on the pins will change at the rate set by FT_SetBaudRate
FT_GetBitMode	FT_GetBitMode returns the instantaneous value of the pins. A single byte will be returned containing the current values of the pins, both those which are inputs and those which are outputs.



AN_232R-01 Bit Bang Mode Availability for the FT232R and FT245R Version 2.03

Document No.: FT_000339 Clearance No.: FTDI# 169

FT_Read

FT_Read will return a buffer of values which have been sampled from the pins at the rate set by FT_SetBaudRate. If the read buffers have filled, data will be lost. Each byte returned contains the values of the pins, both those which are inputs and those which are outputs.

Table 3.4 D2XX Commands

Full descriptions of these functions are available in the <u>D2XX Programmer's Guide</u>.

Code examples can be downloaded from Sample Project

4 CBUS Bit Bang Mode

The FT232R supports a new type of Bit Bang mode on the CBUS pins. The CBUS Bit Bang mode must be configured in the FT232R EEPROM (this can be done using the FT_PROG utility) and then enabled with an FT_SetBitMode command to function. It is not available on the FT245R.

When CBUS Bit Bang mode is enabled the CBUS pins are configured as follows:

FT232RL/FT245RL Pin Number	FT232RQ/FT245RQ Pin Number	Signal	Туре	Description
23	22	C0	Input/Output	Configurable function Bit 0
22	21	C1	Input/Output	Configurable function Bit 1
13	10	C2	Input/Output	Configurable function Bit 2
14	11	C3	Input/Output	Configurable function Bit 3

Table 4.1 CBUS Bit Bang Mode Settings

The FT_SetBitMode and FT_GetBitMode D2XX commands are required to communicate with CBUS Bit Bang. Since these functions allow only a single byte to be sent or received, this version of Bit Bang is much slower than the Asynchronous and Synchronous Bit Bang types when used to transfer large buffers of data with FT_Write and FT_Read, but it does provide an additional 4 IO pins for the FT232R. The data transfer rate is limited by USB frames.

The D2XX commands required to use CBUS Bit Bang mode are listed below:

D2XX Function	Description
FT_SetBitMode	Used to set the CBUS pins as input or output and set them high or low.
FT_GetBitMode	Used to read the value of the CBUS pins.

Table 4.2 D2XX Command

For example:

Set all pins to output with bit 0 high: FT SetBitMode(Handle, 0xF1, 0x20)

Set bits 0 and 1 to input, bits 2 and 3 to output and make bits 2 and 3 high: FT_SetBitMode(Handle, 0xCC, 0x20)

Read pins:

FT GetBitMode(Handle, Data) where the lower nibble is given by (Data AND 0x0F)

Full descriptions of these functions are available in the D2XX Programmer's Guide.

Code examples can be downloaded from Sample Project.



5 Contact Information

Head Office - Glasgow, UK

Future Technology Devices International Limited Unit 1, 2 Seaward Place, Centurion Business Park Glasgow G41 1HH

United Kingdom

Tel: +44 (0) 141 429 2777 Fax: +44 (0) 141 429 2758

E-mail (Sales) sales1@ftdichip.com
E-mail (Support) support1@ftdichip.com
E-mail (General Enquiries) admin1@ftdichip.com

Branch Office - Taipei, Taiwan

Future Technology Devices International Limited (Taiwan)

2F, No. 516, Sec. 1, NeiHu Road

Taipei 114 Taiwan , R.O.C.

Tel: +886 (0) 2 8797 1330 Fax: +886 (0) 2 8751 9737

Branch Office - Tigard, Oregon, USA

Future Technology Devices International Limited

(USA)

7130 SW Fir Loop Tigard, OR 97223-8160

USA

Tel: +1 (503) 547 0988 Fax: +1 (503) 547 0987

E-Mail (Sales) <u>us.sales@ftdichip.com</u>
E-Mail (Support) <u>us.support@ftdichip.com</u>
E-Mail (General Enquiries) us.admin@ftdichip.com

Branch Office - Shanghai, China

Future Technology Devices International Limited

(China)

Room 1103, No. 666 West Huaihai Road,

Shanghai, 200052

China

Tel: +86 21 62351596 Fax: +86 21 62351595

Web Site

http://ftdichip.com

System and equipment manufacturers and designers are responsible to ensure that their systems, and any Future Technology Devices International Ltd (FTDI) devices incorporated in their systems, meet all applicable safety, regulatory and system-level performance requirements. All application-related information in this document (including application descriptions, suggested FTDI devices and other materials) is provided for reference only. While FTDI has taken care to assure it is accurate, this information is subject to customer confirmation, and FTDI disclaims all liability for system designs and for any applications assistance provided by FTDI. Use of FTDI devices in life support and/or safety applications is entirely at the user's risk, and the user agrees to defend, indemnify and hold harmless FTDI from any and all damages, claims, suits or expense resulting from such use. This document is subject to change without notice. No freedom to use patents or other intellectual property rights is implied by the publication of this document. Neither the whole nor any part of the information contained in, or the product described in this document, may be adapted or reproduced in any material or electronic form without the prior written consent of the copyright holder. Future Technology Devices International Ltd, Unit 1, 2 Seaward Place, Centurion Business Park, Glasgow G41 1HH, United Kingdom. Scotland Registered Company Number: SC136640

Appendix A - References Document References

FT232R Product Page

FT232R Datasheet

FT245R Product Page

FT245R Datasheet

D2XX Drivers

D2XX Programmer's Guide

Sample Project

FT PROG Utility

Acronyms and Abbreviations

Terms	Description
EEPROM	Electrically Erasable Programmable Read Only Memory



Appendix B – List of Tables and Figures List of Tables

Table 2.1 Asynchronous Bit Bang Mode IO Configurations	3
Table 2.2 CBUS Pins Settings	3
Table 2.3 D2XX Commands	4
Table 3.1 Synchronous Bit Bang Timing	5
Table 3.2 Synchronous Bit Bang Mode IO Configurations	6
Table 3.3 EEPROM CBUS Pins Settings	6
Table 3.4 D2XX Commands	7
Table 4.1 CBUS Bit Bang Mode Settings	8
Table 4.2 D2XX Command	8
List of Figures	
Figure 3.1 Synchronous Rit Rang Timing Diagram	5

Appendix C - Revision History

Document Title: AN_232R-01 Bit Bang Mode Availability for the FT232R and FT245R

Document Reference No.: FT_000339
Clearance No.: FTDI# 169

Product Page: http://www.ftdichip.com/FTProducts.htm

Document Feedback: Send Feedback

Revision	Changes	Date
Version 1.00	Initial Release	December, 2005
Version 2.00	Reformatted Added a note 1 in section 2	2010-09-06
Version 2.01	Corrected table 2.3 and 3.4. Asynchronous should be: 0x1 synchronous should be: 0x4	2010-10-28
Version 2.02	Corrected section 3 and table 3.4 Asynchronous text changed to synchronous text Data transfer rate (9600 baud) corrected from 6.5ms to 6.5µs (table 3.4 and 2.3) Updated legal disclaimer	2010-11-26
Version 2.03	Changes made to Bitbang WR# strobe CBUS availability. FT_PROG references added.	2018-07-02